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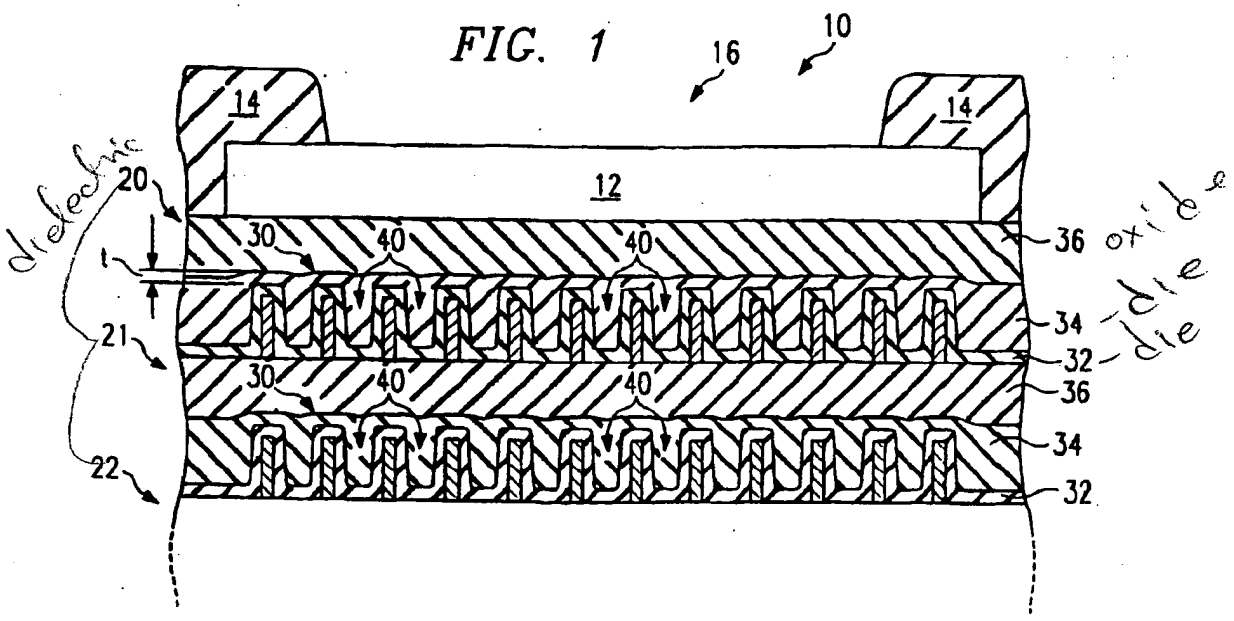
(54) System and method for reinforcing a bond pad

(57) The reinforcing system (10, 70, 90) for a bond pad (12, 72, 92) includes at least one dielectric layer or stack (20, 21, 22, 76, 78, 96, 98) disposed under the bond pad (12, 72, 92). A reinforcing patterned structure (30, 80, 82, 100, 102) is disposed in the dielectric layer or stack (20, 21, 22, 76, 78, 96, 98).

FIG. 1



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Description

TECHNICAL FIELD OF THE INVENTION

This invention is related in general to the field of semiconductor devices and processes. More particularly, the invention is related to system and method for reinforcing a bond pad.

BACKGROUND OF THE INVENTION

A well known problem area in semiconductor processing is the process of attaching a solder, wire or other bonding elements to a bond pad on a semiconductor integrated circuit. These bond pads are typically disposed above one or more layers or stacks of brittle and/or soft dielectric materials, typically oxide of silicon and some organic materials, for planarization and insulation purposes. Some dielectric materials, such as hydrogen silsesquioxane (HSQ), aerogels, organic polyimides, and parylenes are advantageous for their low dielectric constants compared to silicon oxides, but are weaker structurally and mechanically.

During the bonding process, mechanical loading and ultrasonic stresses applied by the bonding capillary tip to the bond pad often result in fracture of the underlying dielectrics, deformation of the underlying metal structures, and delamination of the layers in the metal structures. These bonding failures may appear as craters in the bond pad and underlying layers as the bonding capillary tip is pulled away from the bonding pad. However, these defects often are not apparent during bonding but would manifest themselves during subsequent bond pull and shear tests, reliability tests such as thermal cycle or thermal shock, or upon deprocessing and cross-sectioning.

Further, weakness of the bond pad structure may also reveal themselves during wafer probing prior to bonding. Again, the stresses exerted by the probe tips, typically formed of a hard metal such as tungsten, can cause localized fractures in the pads, despite the fact that they make contact with a soft metal (aluminum), on the bond pads. Such fractures are as much of a reliability hazard as those caused during bonding.

Traditionally, the bonding failures have been addressed by altering bonding parameters, such as ultrasonic power and pulse waveform, bonding temperature, bonding time, clamping force, shape of the bonding capillary tip, etc. Much time is spent experimenting with parameter settings and combinations thereof. Although general guidelines of parameter setpoints and configurations have been developed, the bonding failures persist at a sufficiently significant level to continually threaten the reliability of integrated circuit devices. Yet the failure levels are low such that bonding failures become apparent only after several tens of thousands of devices are bonded.

Recent technological advances in semiconductor processing do not alleviate the situation. New dielectric materials with lower dielectric constants are being used to increase circuit speeds but they are mechanically weaker than the conventional plasma enhanced chemical vapor deposition (CVD) dielectrics. Decreasing bond pad dimensions necessitates the increase of vertical bonding force or forces attributable to the use of ultrasonic energy to form effective bonds. Inaccessibility of higher bond parameter settings for fear of damage to the bond pads also results in longer bond formation time, and consequently, lost throughput. All these significant changes point to a trend of more severe failures and increase in their frequency.

SUMMARY OF THE INVENTION

Accordingly, there is a need for a reliable way to prevent or minimize the occurrence of probe and bonding failures where bond pads are situated above one or more structurally and mechanically weak dielectric layers.

In accordance with the present invention, a bond pad reinforcing system and method are provided which eliminate or substantially reduce the disadvantages associated with prior apparatus and methods.

In one aspect of the invention, the reinforcing system for a bond pad includes a reinforcing patterned structure disposed in at least one dielectric stack disposed under the bond pad.

In another aspect of the invention, the reinforcing system for a bond pad includes at least one dielectric layer or a stack of multiple dielectric layers disposed under the bond pad. A reinforcing patterned structure is disposed in at least one dielectric stack.

In yet another aspect of the invention, a method for reinforcing a bond pad in a semiconductor integrated circuit includes the steps of forming a metal layer, patterning the metal layer in a predetermined area into a predetermined pattern having a plurality of vacant areas, and forming a dielectric layer above the patterned metal layer, filling the vacant areas in the patterned metal layer. A bond pad is then formed on the dielectric layer above the patterned metal layer.

In another aspect of the invention, the reinforcing patterned structure may be a joined or interconnected structure. In another aspect of the invention, the reinforcing patterned structure may comprise disjoined or non-interconnected and repeating elements.

A technical advantage of the present invention is the improved structural integrity of bond pads so that forces exerted during bonding and probing do not damage the bond pad and underlying structures. These technical advantages are possible without changing bonding or probing parameters, which may decrease process throughput. The result is a more reliable integrated circuit and decreasing bonding failures.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference may be made to the accompanying drawings, in which:

FIGURE 1 is a cross-sectional view of an embodiment of a bond pad reinforcing structure according to the teachings of the present invention;

FIGURE 2 is a plan view of the bond pad reinforcing structure in FIGURE 1 according to the teachings of the present invention;

FIGURE 3 is a cross-sectional view of another embodiment of a bond pad reinforcing structure according to the teachings of the present invention;

FIGURES 4A and 4B are plan views of the bond pad reinforcing structure in FIGURE 3 according to the teachings of the present invention;

FIGURE 5 is a cross-sectional view of another embodiment of a bond pad reinforcing structure according to the teachings of the present invention;

FIGURE 6 is a plan view of the bond pad reinforcing structure in FIGURE 5 according to the teachings of the present invention; and

FIGURES 7-11 are further plan views of varying embodiments of the bond pad reinforcing structure according to the teachings of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the present invention are illustrated in FIGURES 1-11, like reference numerals being used to refer to like and corresponding parts of the various drawings.

Referring to FIGURE 1, a reinforcing structure 10 for a bond pad 12 is shown. A center portion 16 of bond pad 12 is exposed and uncovered from a protective oxide layer 14 for receiving a ball bond (not shown), typically constructed from aluminum, gold, copper, solder, or like materials. Bond pad 12 is typically a multi-layered stack constructed of aluminum and one or more layers of titanium nitride and titanium, for example. Underlying bond pad 14 is one or more intermetal dieletric layers or one or more dielectric stacks 20-22, each constructed of multiple dielectric layers. Each intermetal dielectric layer or stack 20-22 may include a reinforcing grid 30 disposed in at least one of the intermetal dielectric stacks 20-22. FIGURE 2 shows a plan view of reinforcing grid 30, which has a regular repeating pattern with a plurality of voids or vacant areas.

At least one layer of the intermetal dielectric materials within each dielectric layer or stack 20-22 is constructed of a mechanically and structurally weak dielectric material, such as oxide, hydrogen silsesquioxane (HSQ), Aerogels, organic polyimides, parylenes, and the like. These dielectric materials are hereinafter referred to generally as weak dielectric materials. Each intermetal dielectric stack 20-22 may include, for example, a first dielectric layer 32, a weak dielectric layer 34, and a second dielectric layer 36. Dielectric layers 32 and 36 may be TEOS (tetraethyl orthosilicate) or any other oxide material formed by a suitable method. It may be seen that by providing a reinforcing structure 30 of a predetermined height, the thickness, t, of weak dielectric layer 34 atop reinforcing structure 30 is greatly reduced. Further, reinforcing structure 30 is a joined or interconnected grid structure with a plurality of voids or vacant areas 40 for containing and accommodating a large portion of weak dielectric material 34 therein. Accordingly, reinforcing structure 30 provides support and mechanical strength to intermetal dielectric stacks 20-22 to substantially decrease the incidents of cratering and other bonding failures caused by wire bonding.

It may be seen from FIGURES 1 and 2 that reinforcing structure 30 is generally planar with a thickness less than the desired thickness of intermetal dielectric stacks 20-22. Further, reinforcing structure 30 is preferably dimensioned to fit generally within and not significantly extending beyond an area defined by bond pad 12. When more than one reinforcing layer is used, reinforcing structure 30 for each intermetal dielectric stack 20-22 may be aligned directly above one another, as shown, or be offset with one another. It is contemplated that any number, including one, of reinforcing structures or layers may be used to achieve improved structural integrity and robustness. It is also contemplated that intermetal dielectric layers or stacks 20-22 may include reinforcing structures of different patterns, although such designs may require additional expense to use different masks to pattern etch the different metal reinforcing structures.

Bond pad reinforcing structure 10 may be constructed by forming a layer of metal or any suitable conductor or semiconductor of predetermined thickness at the start of each intermetal dielectric layer or stack 20-22. The reinforcing layer is then pattern etched into the desired pattern, such as the grid pattern shown in FIGURES 1 and 2. Subsequent dielectric materials are then formed above the patterned reinforcing layer, such as a single dielectric layer or oxide layer 32, weak dielectric layer 34, and oxide layer 36 as shown. Note that weak dielectric layer 34 may be formed by a number of methods, including spin-on, plasma enhanced chemical vapor deposition (CVD), and vapor condensation.

Referring to FIGURES 3, 4A, and 4B, another embodiment of bond pad reinforcing structure 70 is shown. A bond pad 72 is disposed below a protective overcoat of oxide 74 and partially exposed for wire/solder/flip-chip/wedge bonding. Two intermetal dielectric stacks 76 and 78 underlying bond pad 72 include reinforcing structures 80 and 82. Reinforcing structures 80 and 82 include a repeating and non-interconnected pattern such as the crucifix pattern shown arranged in a regular manner. It may be seen that reinforcing structure 80 and 82 may be slightly offset from one another as shown. The semiconductor integrated circuit may include one, two, or more than two intermetal dielectric layers or stacks

FIG. 1

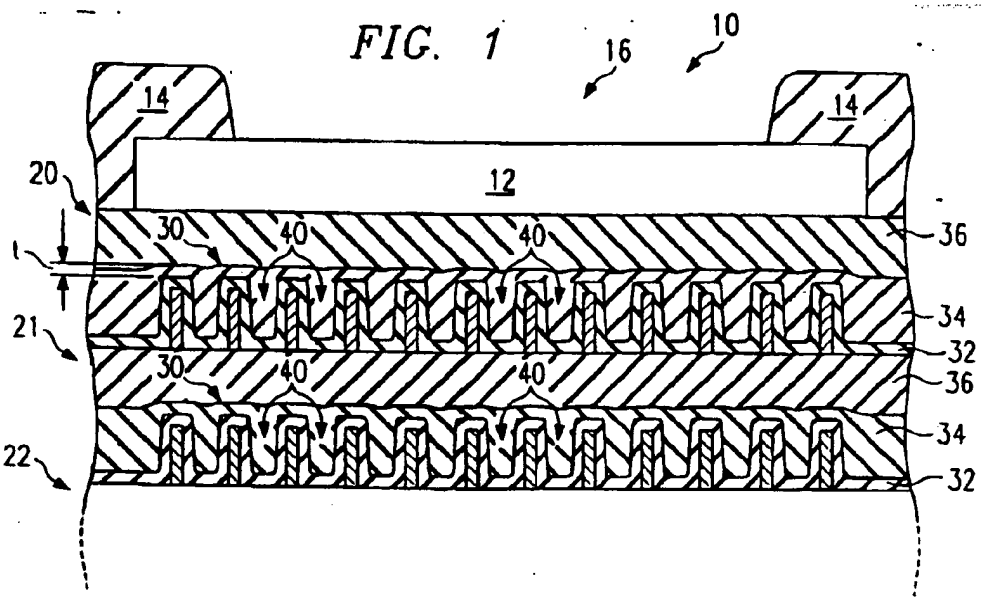

FIG. 2

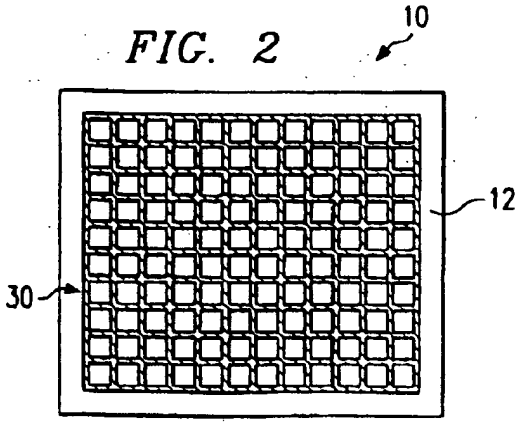

FIG. 4A

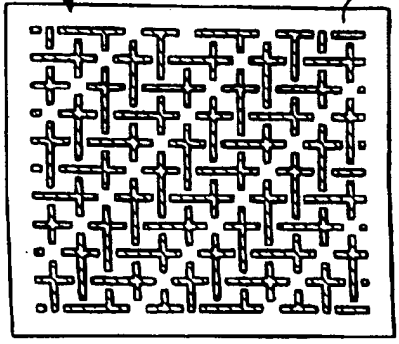

FIG. 4B

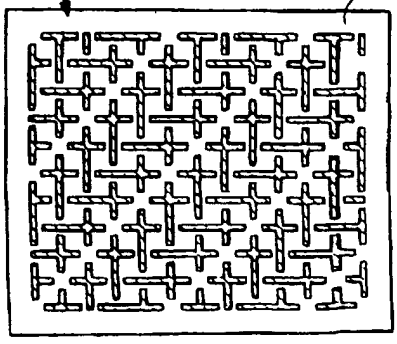

FIG. 3

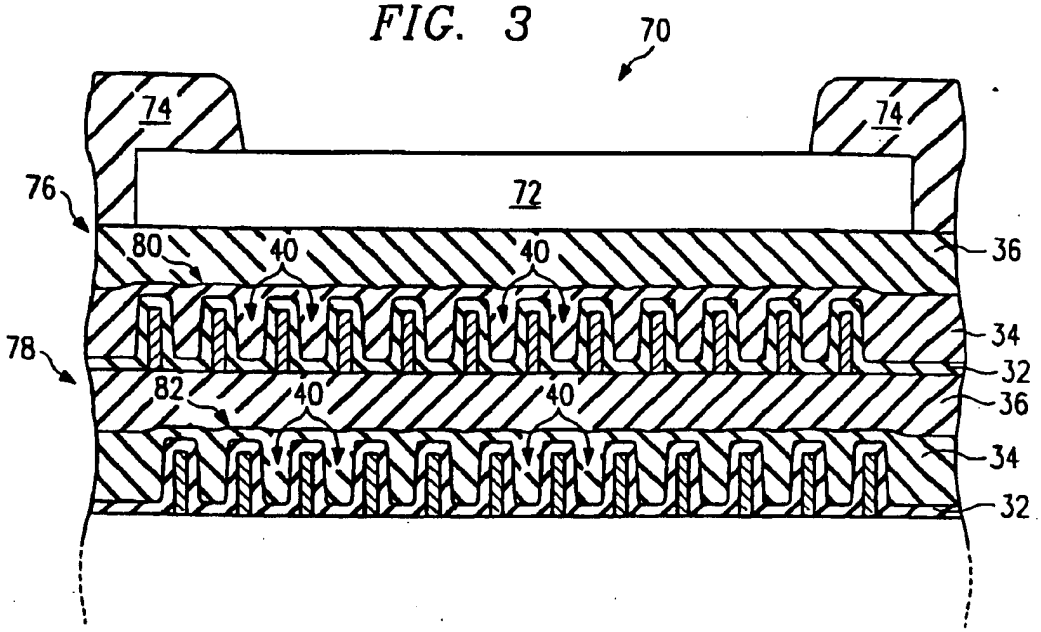
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FIG. 5

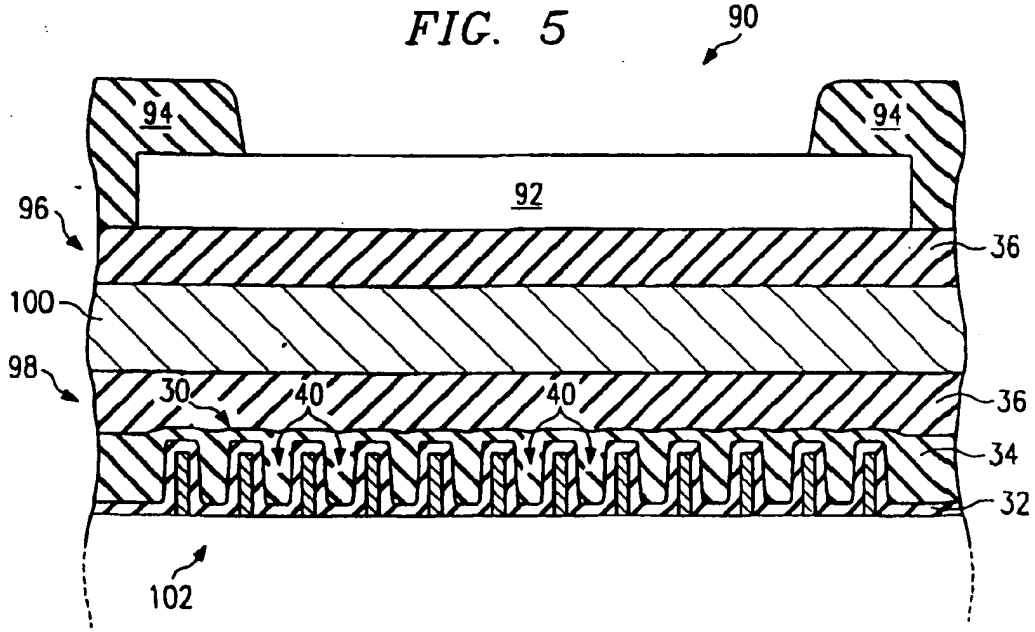
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FIG. 6

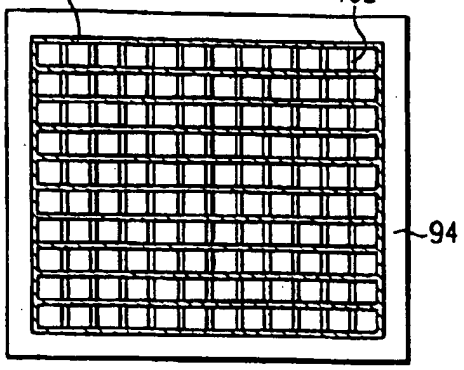

FIG. 7

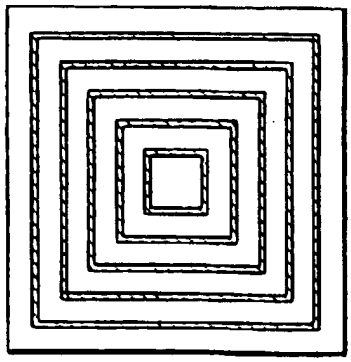

FIG. 8

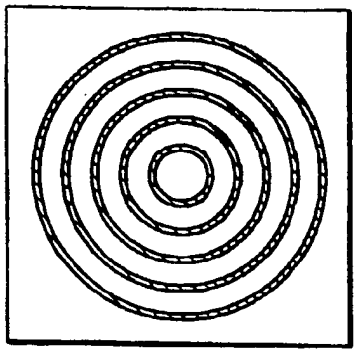

FIG. 9

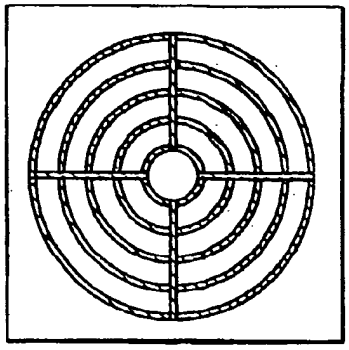

FIG. 10

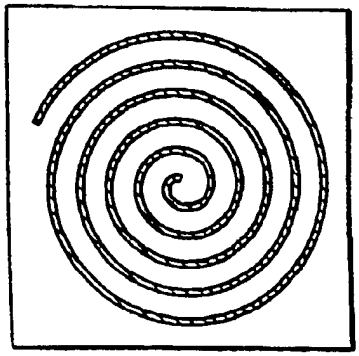

FIG. 11